UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/475,717	12/30/1999	MARK D. NARDIN	042390.P6942	6762

7590 02/18/2004

GLENN E VON TERSCH
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD 7TH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	14

DATE MAILED: 02/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/475,717	Applicant(s) NARDIN ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *2,7,13,19,21,23,25 and 27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-6, 8-12, 14-18, 20, 22, 24, 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 21, 23, 25 and 27 have been cancelled and withdrawn from consideration as per Applicant's request. Claims 1, 3, 4, 5, 6, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 20, 22, 24 and 26 have been presented for reconsideration in light of Applicants amended claim language. Claims 1, 3, 4, 5, 6, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 20, 22, 24 and 26 have been reconsidered and are rejected.

Response to Arguments

2. Regarding Applicants submission of an affidavit under 37 C.F.R. 1.131:

The affidavit filed on 12-09-2003 under 37 CFR 1.131 has been considered but is ineffective to overcome the *Sinha et al.* reference.

The evidence submitted is insufficient to establish a reduction to practice of the invention in this country or a NAFTA or WTO member country prior to the effective date of the November 1999 reference. As regards the claimed limitation of *"indicating whether any of the domino logic circuits is likely to generate an erroneous output"*, it is unclear to the Examiner exactly where in the Applicant's Exhibits A or B this claimed limitation is disclosed.

The MPEP in section 715.07:

> The affidavit or declaration and exhibits must clearly explain which facts or data applicant is relying on to show completion of his or her invention prior to the particular date. Vague and general statements in broad terms about what the exhibits describe along with a general assertion that the exhibits describe a reduction to practice ''amounts essentially to mere pleading, unsupported by proof or a showing of facts'' and, thus, does not satisfy the requirements of 37 CFR 1.131(b). In re Borkowski, 505 F.2d 713, 184 USPQ 29 (CCPA 1974). Applicant must give a clear explanation of the exhibits pointing out exactly what facts are established and relied on by applicant. 505 F.2d at 718-19, 184 USPQ at 33. See also In re Harry, 333 F.2d 920, 142 USPQ 164 (CCPA 1964) (Affidavit ''asserts that facts exist but does not tell what they are or when they occurred'').

The Examiner requires a clear mapping of where in the Applicant's exhibits the claimed limitation, *"indicating whether any of the domino logic circuits is likely to generate an erroneous output"* is disclosed such that it is clear that this limitation of Applicant's claimed invention was conceived or reduced to practice before the November 1999 reference date.

2.1 It is further noted by the Examiner that only *Mark D. Nardin* has signed the Affidavit. The other inventors *Hans Greub* and *Sapumal Wijeratne* have not signed the Affidavit as required by the MPEP, *see section 715.04.*

715.04 Who May Make Affidavit or Declaration; Formal Requirements of Affidavits and Declarations

WHO MAY MAKE AFFIDAVIT OR DECLARATION
The following parties may make an affidavit or declaration under 37 CFR 1.131:
(A) All the inventors of the subject matter claimed.
(B) An affidavit or declaration by less than all named inventors of an application is accepted where it is shown that less than all named inventors of an application invented the subject matter of the claim or claims under rejection. For example, one of two joint inventors is accepted where it is shown that one of the joint inventors is the sole inventor of the claim or claims under rejection.
(C) A party qualified under 37 CFR 1.42, 1.43, or 1.47 in situation where some or all of the inventors are not available or not capable of joining in the filing of the application.
(D) The assignee or other party in interest when it is not possible to produce the affidavit or declaration of the inventor. Ex parte Foster, 1903 C.D. 213, 105 O.G. 261 (Comm'r Pat. 1903.
Affidavits or declarations to overcome a rejection of a claim or claims must be made by the inventor or inventors of the subject matter of the rejected claim(s), a party qualified under 37 CFR 1.42, 1.43, or 1.47, or the assignee or other party in interest when it is not possible to produce the affidavit or declaration of the inventor(s). Thus, where all of the named inventors of a pending application are not inventors of every claim of the application, any affidavit under 37 CFR 1.131 could be signed by only the inventor(s) of the subject matter of the rejected claims. Further, where it is shown that a joint inventor is deceased, refuses to sign, or is otherwise unavailable, the signatures of the remaining joint inventors are sufficient. However, the affidavit or declaration, even though signed by fewer than all the joint inventors, must show completion of the invention by all of the joint inventors of the subject matter of the claim(s) under rejection. In re Carlson, 79 F.2d 900, 27 USPQ 400 (CCPA 1935).

2.2 It is further noted that the inventor listed in Applicant's exhibit A is *Hans J. Greub, see page 1 of Exhibit A,* and yet inventor *Mark D. Nardin* signed Applicants affidavit. It is unclear to the Examiner as to which inventor reduced to practice the invention as disclosed in the Affidavit.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1, 3, 4, 5, 6, 8, 9, 18 and 20** are rejected under **35 U.S.C. 103(e)** as being unpatentable over **Rajgopal et al. U.S. Patent 6,363,515** in view of **Beausang U.S. Patent 5,828,579** and in further view of **"Validation and Test Generation for Oscillatory Noise in VLSI Interconnects" by Arani Sinha, Sandeep K. Gupta and Melvin A. Breuer** hereafter referred to as the *Sinha et al.* reference.

3.1 As regards independent **Claims 1 and 4** the *Rajgopal et al.* reference discloses simulating each domino circuit of a set of domino circuits **(Col. 3 Lines 65-67 and Col. 4 Lines 1-22),** and reporting the results **(Figure 1, Col. 7 Lines 26-39)** and discloses domino logic circuit having a set of inputs and an output and simulating each domino logic circuit after any circuits coupled to the set of inputs have been simulated, **(Col. 2 Lines 15-20 and Col. 3 Lines 58-65).** The *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

However, the *Rajgopal et al.* reference does not expressly disclose the limitation concerning analysis of domino circuits wherein each domino circuit is simulated in a specific order and the next domino circuit is analyzed using as an input the output of the last domino circuit that was analyzed and reporting results of the simulation indicating whether any of the domino logic circuits are likely to generate an erroneous output.

The *Beausang* reference discloses an analysis of circuits wherein the circuit is simulated in a specific order and next circuit analyzed is using the output of the last circuit that was analyzed according to an ordered list, **(Figures 6A, 6B, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12A, 12B, 12C, 13A, 13B, 14A, 14B, Col. 3 Lines 1-12, Lines 58-67, Col. 4 Lines 1-15, Col. 21 Lines 10-34, Col. 39 Lines 46-67, Col. 40 Lines 1-7).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Beausang* reference because *(motivation to combine)* the *Beausang* reference discloses a method wherein a user can modify a complex design, enter very specific design constraints and then verify a complex design in less time ***(Beausang Col. 2 Lines 21-67, Col. 3 Lines 1-12).***

The *Sinha et al.* reference discloses reporting results of the simulation indicating whether any of the domino logic circuits are likely to generate an erroneous output **(pp. 293 Procedure for Test Generation & pp.294 Test Generation Example).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Rajgopal et al.* reference with the *Sinha et al.* reference because, the inductance of on-chip interconnects can lead to high levels of noise and there exists a need to test and validate a design to make certain that the noise magnitude stays below a level that will support proper chip functionality ***(Sinha et al. pp. 296 Conclusions).***

3.2 As regards **Claim 3** the *Rajgopal et al.* reference discloses simulating each domino logic circuit including the simulated results of circuits coupled to the inputs of the domino logic circuit **(Col. 3 Lines 58-67, Col. 4 Lines 1-8).**

3.3 As regards **Claim 5** the *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

3.4 As regards **Claim 6** the *Rajgopal et al.* reference discloses a reporting of the results of the simulation, **(Figure 1, Col. 7 Lines 26-39).**

3.5 As regards **Claim 8** the *Rajgopal et al.* reference discloses extracting parameters **(Figure 1 Item 22),** an ordered list **(Figure 6 Item 72, Figure 5 and Figure 4)** the Examiner asserts that a NETLIST is an ordered list, and simulating non-domino circuits **(Figure 6 Item 81)** the Examiner asserts that the buffers being inserted are not, in and of themselves domino circuits.

3.6 As regards **Claim 9** the *Rajgopal et al.* reference discloses simulating non-domino circuits **(Figure 6 Item 81)** the Examiner asserts that the buffers being inserted are not, in and of

themselves domino circuits, and reporting the results of simulating the non-domino circuits **(Figure 1, Col. 7 Lines 26-39).**

3.7 As regards dependent **Claims 18 and 20** the *Rajgopal et al.* reference does not expressly disclose determining *worst-case noise.*

The *Sinha et al.* reference discloses *worst-case noise* **(pp. 293 Procedure for Test Generation).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Rajgopal et al.* reference with the *Sinha et al.* reference because, the inductance of on-chip interconnects can lead to high levels of noise and there exists a need to test and validate a design to make certain that the noise magnitude stays below a level that will support proper chip functionality ***(Sinha et al. pp. 296 Conclusions).***

4. **Claims 10, 11, 12, 14, 15, 16, 17, 22, 24 and 26** are rejected under **35 U.S.C. 103(e)** over **Rajgopal et al. U.S. Patent 6,363,515** in view of and in further view of **Beausang U.S. Patent 5,828,579** and in further view of **Conn et al. U.S. Patent 5,999,714** and in further view of **"Validation and Test Generation for Oscillatory Noise in VLSI Interconnects" by Arani Sinha, Sandeep K. Gupta and Melvin A. Breuer** hereafter referred to as the *Sinha et al.* reference.

4.1 As regards independent **Claims 10, 15 and 17** the *Rajgopal et al.* reference discloses simulating each domino circuit of a set of domino circuits **(Col. 3 Lines 65-67 and Col. 4 Lines 1-22),** and reporting the results **(Figure 1, Col. 7 Lines 26-39)** and discloses domino logic circuit having a set of inputs and an output and simulating each domino logic

circuit after any circuits coupled to the set of inputs have been simulated, **(Col. 2 Lines 15-20 and Col. 3 Lines 58-65).** The *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

However, the *Rajgopal et al.* reference does not expressly disclose the limitation concerning analysis of domino circuits wherein each domino circuit is simulated in a specific order and the next domino circuit is analyzed using as an input the output of the last domino circuit that was analyzed and reporting results of the simulation indicating whether any of the domino logic circuits are likely to generate an erroneous output.

The *Beausang* reference discloses an analysis of circuits wherein the circuit is simulated in a specific order and next circuit analyzed is using the output of the last circuit that was analyzed according to an ordered list, **(Figures 6A, 6B, 7A, 7B, 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12A, 12B, 12C, 13A, 13B, 14A, 14B, Col. 3 Lines 1-12, Lines 58-67, Col. 4 Lines 1-15, Col. 21 Lines 10-34, Col. 39 Lines 46-67, Col. 40 Lines 1-7).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Beausang* reference because *(motivation to combine)* the *Beausang* reference discloses a method wherein a user can modify a complex design, enter very specific design constraints and then verify a complex design in less time ***(Beausang Col. 2 Lines 21-67, Col. 3 Lines 1-12).***

The *Sinha et al.* reference discloses reporting results of the simulation indicating whether any of the domino logic circuits are likely to generate an erroneous output **(pp. 293 Procedure for Test Generation & pp.294 Test Generation Example).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Rajgopal et al.* reference with the *Sinha et al.* reference because, the inductance of on-chip interconnects can lead to high levels of noise and there exists a need to test and validate a design to make certain that the noise magnitude stays below a level that will support proper chip functionality ***(Sinha et al. pp. 296 Conclusions).***

4.2 As regards **Claim 10** the *Rajgopal et al.* reference does not expressly disclose a machine-readable medium.

The *Conn et al.* reference discloses a machine-readable medium **(Col. 2 Lines 22-42).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Conn et al.* reference because *(motivation to combine)* the *Conn et al.* reference discloses a method of taking into consideration noise and performing circuit optimization that results in greater design efficiency ***(Conn et al. Col. 4 Lines 29-47).***

4.3 As regards **Claim 15** the *Rajgopal et al.* reference does not expressly disclose a processor, a memory controller coupled to the processor, and a memory coupled to the memory controller.

The *Conn et al.* reference discloses a processor, a memory controller coupled to the processor, and a memory coupled to the memory controller **(Col. 2 Lines 22-42).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Conn et al.* reference because *(motivation to combine)* the *Conn et al.* reference discloses a method of taking into consideration noise and

performing circuit optimization that results in greater design efficiency ***(Conn et al. Col. 4 Lines 29-47).***

4.4 As regards **Claim 17** the *Rajgopal et al.* reference does not expressly disclose an apparatus.

The *Conn et al.* reference discloses an apparatus **(Col. 2 Lines 22-42).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rajgopal et al.* reference with the *Conn et al.* reference because *(motivation to combine)* the *Conn et al.* reference discloses a method of taking into consideration noise and performing circuit optimization that results in greater design efficiency ***(Conn et al. Col. 4 Lines 29-47).***

4.5 As regards **Claims 11 and 16** the *Rajgopal et al.* reference discloses parameter extraction **(Figure 1 Item 22).**

4.6 As regards to **Claim 12** the *Rajgopal et al.* reference discloses reporting results **(Figure 1, Col. 7 Lines 26-39).**

4.7 As regards **Claim 14** the *Rajgopal et al.* reference discloses an ordered list **(Figure 6 Item 72, Figure 5 "Block Netlist for Adder")** the Examiner asserts that a NETLIST is an ordered list. The *Rajgopal et al.* reference discloses extracting parameters **(Figure 1 Item 22),** and simulating non-domino circuits **(Figure 6 Item 81)** the Examiner asserts that the buffers being inserted are not, in and of themselves domino circuits.

4.8 As regards dependent **Claims 22, 24 and 26** the *Rajgopal et al.* reference does not expressly disclose determining worst-case noise.

The *Sinha et al.* reference discloses *worst-case noise* **(pp. 293 Procedure for Test Generation).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Rajgopal et al.* reference with the *Sinha et al.* reference because, the inductance of on-chip interconnects can lead to high levels of noise and there exists a need to test and validate a design to make certain that the noise magnitude stays below a level that will support proper chip functionality ***(Sinha et al. pp. 296 Conclusions).***

Conclusion

5. Claims 1, 3-6, 8-12, 14-17, 20, 22, 24 and 26 are rejected.

5.1 THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

HUGH JONES PH.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100